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EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,409	JOHNSON, BRIAN D.	
	Examiner	**Art Unit**	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-20* is/are rejected.

7)☒ Claim(s) *6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/13/2004*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 and 18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 18 of copending Application No. 10/779,408 in view of Ellersick et al., U.S. Patent No. 6,044,122. All claim limitations in Ellersick are disclosed in Figures 1-10.

Claim 1 in copending Application No. 10/779,408 discloses an integrating circuit including all claim limitations of claim 1 in the current Application except each delay element having an input, a first selection circuit coupled to a plurality of inputs of the first series of delay elements, a phase detector coupled to an output of the selection circuit, and a delay circuit coupled to the counter.

Ellersick teaches a digital delay-locked loop 42 including a delay elements 106a-f, each delay element having an input (68 and 110a-f), a first selection circuit 108

coupled to a plurality of inputs of the first series of delay elements (FIG. 4), a phase detector 88 coupled to an output of the selection circuit (output 43a from MUX 108 propagates though 70b-h to connect to input D on PHASE DETECTOR 88, FIG(s) 3 and 4), and a delay circuit 70a-h coupled to the counter 96 (through DECODER 102). In Ellersick, the described circuit arrangement is used for rapidly acquiring the signal phase of an incoming data signal (column 2, lines 38-40) where accuracy is achieved without expensive digital clock recovery circuits (column 2, lines 20-27) Thus, the implementation cost is reduced (column 2, lines 32-34).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above described circuit arrangement, as suggested by Ellersick with the integrated circuit integrated circuit disclosed in claim 1 of copending Application No. 10/779,408 in order to implement each delay element having an input, a first selection circuit coupled to a plurality of inputs of the first series of delay elements, a phase detector coupled to an output of the selection circuit, and a delay circuit coupled to the counter. One of ordinary skill in the art would be motivated to do so in order to reduce implementation cost.

Claim 18 in copending Application No. 10/779,408 discloses an integrating circuit including all claim limitations of claim 18 in the current Application except delaying the reference clock signal using a first number of delay elements, each delay element providing a delayed reference clock signal, selecting one of the delayed reference clock signals, and delaying the data strobe signal using a second number of delay elements.

Ellersick teaches a digital delay-locked loop 42 where the reference clock 31 is delayed by a first number of delay elements 70a (column 5, lines 15-17, lines 19-22,

lines 24-29, FIG. 3), each delay element 110a-f providing a delayed reference clock signal (column 6, lines 48-58), selecting one of the delayed reference clock signals (column 6, line 65 – column 7, line 10), and delaying the signal using a second number of delay elements 70b (second number of delay elements 116a-f within 70b – column 6, lines 45-47, column 7, line 56 – column 8, line 9, FIG. 5). In Ellersick, the described circuit arrangement is used for rapidly acquiring the signal phase of an incoming data signal (column 2, lines 38-40) where accuracy is achieved without expensive digital clock recovery circuits (column 2, lines 20-27) Thus, the implementation cost is reduced (column 2, lines 32-34).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above described circuit arrangement, as suggested by Ellersick with the integrated circuit integrated circuit disclosed in claim 18 of copending Application No. 10/779,408 in order to implement each delay element having an input, a first selection circuit coupled to a plurality of inputs of the first series of delay elements, a phase detector coupled to an output of the selection circuit, and a delay circuit coupled to the counter. One of ordinary skill in the art would be motivated to do so in order to reduce implementation cost.

Drawings

The drawings are objected to because Figures 1-22 contain hand written text, which is hard to read (e.g. Fig(s) 4, 14, and 22). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if

only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 10, 15, and 18 are objected to because of the following informalities:

The dependency of claims 10 and 15 appears to be wrong. For examination purposes, claim 10 depends on claim 9 and claim 15 depends on claim 14 (see attached Interview Summary with applicant's representative dated 06/29/2006). In addition, the dependency of claims 11, 16, and 17 was changed to claim 9 (per applicant's representative request during the same interview on 06/29/2006).

In claim 18, line 6, the word "to" appears to be missing after the word "phase". In addition, replacing the word "the" with "a" prior of the phrase "plurality of control signals" is suggested in order to avoid the insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9-13, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Ellersick et al., U.S. Patent No. 6,044,122. All claim limitations in Ellersick are disclosed in Figures 1-10.

Regarding claim 1, Ellersick discloses an integrated circuit (column 2, lines 42-45) comprising:

a control block (FIG. 3) comprising:

a first series of delay elements 106a-f coupled to a reference clock input 68, each delay element having an input (column 5, lines 15-17, lines 19-22, lines 24-29, FIG. 3, column 6, lines 48-54, FIG. 4);

a first selection circuit 108 coupled to a plurality of inputs of the first series of delay elements (FIG. 4, 68 and 110a-f);

a phase detector 88 coupled to the reference clock input (REF_CLOCK 31 through synchronizing flip-flop 90, FIG. 3) and an output of the selection circuit (output 43a from MUX 108 propagates though 70b-h to connect to input D on PHASE DETECTOR 88, FIG(s) 3 and 4); and

a counter 96 coupled to the phase detector 88 and the series of delay elements (plurality of delay elements within DELAY ELEMNT 70a, as detailed on

FIG. 4, coupled to UP-DOWN COUNTER 96 though DECODER 102, FIG. 3); and

a delay circuit 70a coupled to the counter 96 (through DECODER 102).

Regarding claim 2, Ellersick further discloses the integrated circuit wherein the first selection circuit comprises a multiplexer 108 (column 6, line 65 – column 7, line 10, FIG. 4).

Regarding claim 3, Ellersick further discloses the integrated circuit wherein the delay circuit comprises:

a second series of delay elements 70b (second series of delay elements 116a-f within 70b – column 6, lines 45-47, column 7, line 56 – column 8, line 9, FIG. 5), each having an input (43a and 120a-f); and

a second selection circuit 118 coupled to a plurality of inputs 120a-f of the second series of delay elements (FIG. 5).

Regarding claim 4, Ellersick further discloses the integrated circuit as per claim 3 wherein an output of the second selection circuit 43h couples to a first storage element 88 (the output of 70h is the output from MUX 118 and DELAY ELEMENT 70h is identical to DELAY ELEMENT 70b – column 6, lines 45-47, FIG. 5).

Regarding claim 5, Ellersick further discloses the integrated circuit as per claim 4 wherein the first storage element is a flip-flop (column 5, lines 63-64).

Regarding claim 9, Ellersick discloses an integrated circuit (column 2, lines 42-45) comprising:

a control circuit (FIG. 3), configured to receive a reference clock 31 and provide plurality of control bits 104a-h (column 5, line 51 – column 6, line 36, column 9, lines 33-41, FIG(s) 3 and 7); and

a delay line 70a configured to receive the plurality of stored control bits 104a-h (column 7, lines 1-10, FIG. 4) wherein the delay line comprises:

a first series of delay elements 106a-f each having an input (FIG. 4); and

a first select circuit 108 configured to a plurality of inputs (68 and 110a-f) of the first series of delay elements.

Regarding claim 10, Ellersick further discloses the integrated circuit wherein the first select circuit is a multiplexer 108 (column 8, line 65 – column 7, line 10).

Regarding claim 11, Ellersick further discloses the integrated circuit wherein the control circuit comprises:

a second series of delay elements 70b (second number of delay elements 116a-f within 70b – column 6, lines 45-47, column 7, line 56 – column 8, line 9, FIG. 5) configured to receive the reference clock (reference clock 31 arriving on line 68 propagates through all delay elements, FIG. 3), each delay element having an input (43a and 120a-f); and

a second select circuit 118 coupled to a polarity of inputs 120a-f of the second series of delay elements (FIG. 5).

Regarding claim 12, Ellersick further discloses the integrated circuit as per claim 11 wherein the control circuit further comprises:

a phase detector 88 configured to compare the phases of the reference clock (reference clock signal 31 is coupled to PHASE DETECTOR for phase comparison

through flip-flop 90, FIG. 3) and an output of second select circuit 43h (the output of 70h is the output from MUX 118 and DELAY ELEMENT 70h is identical to DELAY ELEMENT 70b – column 6, lines 45-47, FIG. 5) and provide an output signal 94; and

a counter 96 configured to receive the phase detector output 94 and provide the control bits (column 5, line 51 – column 6, line 36, column 9, lines 33-41, FIG(s) 3 and 7).

Regarding claim 13, Ellersick further discloses the integrated circuit as per claim 12 wherein a polarity of the phase detector output depends on the relative phase of the reference clock and the output of the second select circuit, and the counter is an up-down counter that counts up when the phase detector output has a first polarity, and counts down when the phase detector output has a second polarity (column 5, line 63 – column 6, line 18).

Regarding claim 16, Ellersick further discloses the integrated circuit, wherein the control circuit is a delay-locked loop (column 2, lines 50-56).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 8, 14, 15, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellersick et al., U.S. Patent No. 6,044,122. All claim limitations in Ellersick are disclosed in Figures 1-10.

Regarding claim 18, Ellersick discloses a method of delaying a data strobe signal comprising:

receiving a reference clock signal 31;

delaying the reference clock signal (column 5, lines 15-17, lines 19-22, lines 24-29, FIG. 3) using a first number of delay elements 70a (first number of delay elements 106a-f within 70a, FIG. 4), each delay element providing a delayed reference clock signal (column 6, lines 48-58);

selecting one of the delayed reference clock signals (column 6, line 65 – column 7, line 10);

comparing the phase of the reference clock signal and the selected delayed reference clock signal to generate a plurality of control signals (column 5, line 51 – column 6, line 36); and

delaying the data strobe signal using a second number of delay elements 70b (second number of delay elements 116a-f within 70b – column 6, lines 45-47, column 7, line 56 – column 8, line 9, FIG. 5).

Ellersick does not specifically state delaying the data strobe signal. The examiner takes Official Notice that delaying data strobe signals is well known in the art. Data

strobe signals (e.g. DQS) require phase shift adjustment such that reliable data transfer is ensured when for example double-data-rate (DDR) memories are accessed. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the method disclosed by Ellersick in order to implement delaying the data strobe signal. One of ordinary skill in the art would be motivated to do so in order to ensure reliable data transfer.

Regarding claim 14, Ellersick further discloses the integrated circuit as per claim 11 wherein the first series of delay elements 70a (FIG. 4) is configured to delay a signal (column 6, lines 54-58).

Similarly to claim 18, Ellersick does not specifically state to delay a read strobe signal. The examiner takes Official Notice that delaying a read strobe signals is well known in the art. Read strobe signals (e.g. DQS) require phase shift adjustment such that reliable data transfer is ensured when for example double-data-rate (DDR) memories are accessed. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the method disclosed by Ellersick in order to implement to delay a read strobe signal. One of ordinary skill in the art would be motivated to do so in order to ensure reliable data transfer.

Regarding claims 8 and 17, Ellersick does not specifically state wherein the integrated circuit is a field programmable gate array. The examiner takes Official Notice that implementing integrated circuits (ICs) with field programmable gate arrays (FPGAs) is well known in the art. FPGAs allow for easily changing the IC's hardware parameters by software, thus providing design flexibility, saving cost and time. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention

to implement the integrated circuit disclosed by Vogt with a field programmable gate array. One of ordinary skill in the art would be motivated to do so in order to provide flexible IC design, save cost and time.

Regarding claim 15, Ellersick further discloses the integrated circuit as per claim 14 further comprising a storage element 88 configured to receive an output of the first select circuit (output 43a from MUX 108 propagates though 70b-h to connect to input D on PHASE DETECTOR 88, FIG(s) 3 and 4).

Regarding claim 19, Ellersick further discloses the method as per calim18 wherein each of the second number of delay elements 70b provide a delayed strobe signal (column 7, line 56 – column 8, line 9, FIG. 5); and the method further comprises selecting one of the delayed strobe signals (column 8, lines 10-24).

Regarding claim 20, Ellersick further discloses the method as per claim 19 further comprising:

receiving a data signal using the selected one of the delayed strobe signals (column 2, line 62 – column 3, line 1).

Allowable Subject Matter

Claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 6, the prior art fails to disclose or suggest the subject matter of claim 4 wherein "an output of the second selection circuit couples to a clock input of a first flip-flop and a complementary clock input of a second clock".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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